

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to current requirements of MIL-PRF-38534.	05-07-26	Raymond Monnin

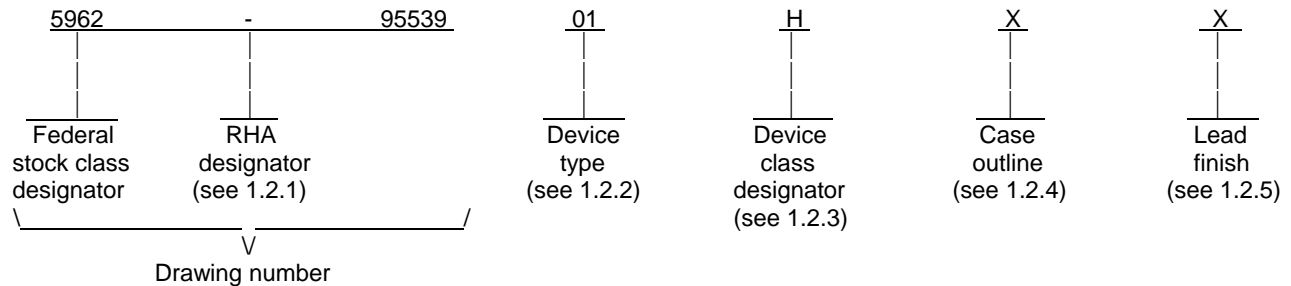
REV	A	A	A	A	A	A	A	A	A	A	A										
SHEET	35	36	37	38	39	40	41	42	43	44	45										
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
REV STATUS OF SHEETS				REV SHEET				A	A	A	A	A	A	A	A	A	A	A	A	A	
								1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Steve L. Duncan		<p align="center">DEFENSE SUPPLY CENTER COLUMBUS POST OFFICE BOX 3990 COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil</p>																		
<p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Michael C. Jones																				
	APPROVED BY Kendall A. Cottongim		<p align="center">MICROCIRCUIT, HYBRID, LINEAR, MIL-STD-1553/1760 PROTOCOL, DUAL REDUNDANT, REMOTE TERMINAL UNIT, +5 VOLT SUPPLY</p>																		
	DRAWING APPROVAL DATE 98-08-06																				
	REVISION LEVEL A																				SIZE A
				SHEET 1 OF 45																	

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	RTM1760	MIL-STD-1553/1760 protocol, dual redundant, +5 volt supply, monolithic transceivers, remote terminal with 4k x 16 RAM
02	RTS1760	MIL-STD-1553/1760 protocol, dual redundant, +5 volt supply, monolithic transceivers, remote terminal with DMA controller

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

<u>Device class</u>	<u>Device performance documentation</u>
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C, and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 2

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	96	Flat package
Y	See figure 1	100	Pin grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. ^{1/}

Supply voltage range (V_{CC})	-0.3 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Lead soldering temperature (10 seconds).....	+265°C
Receiver differential voltage.....	19.0 V p-p
Power dissipation (P_D) $T_C = +125^\circ\text{C}$	680 mA (100% duty cycle)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}).....	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH}).....	+2.2 V dc
Maximum low level input voltage (V_{IL}).....	+0.7 V dc
Case operating temperature range (T_C).....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

^{1/} Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 3

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveform(s). The timing waveform(s) shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 4

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input voltage high <u>2/ 4/</u>	V _{IH}	V _{CC} = 5.5 V, I _{IH} ≤ 30 μA	1,2,3	All	2.2		V
Input voltage low <u>2/ 4/</u>	V _{IL}	V _{CC} = 5.5 V, I _{IL} ≤ 30 μA	1,2,3	All		0.7	V
Low level output current <u>2/ 5/</u>	I _{OL}	V _{CC} = 5.5 V, V _{OL} ≤ 0.4 V	1,2,3	All		±6	mA
High level output current <u>2/ 5/</u>	I _{OH}	V _{CC} = 5.5 V, V _{OH} ≤ 2.7 V	1,2,3	All		±6	mA
Supply current <u>6/</u>	I _{CCA/B}	Standby 25% duty cycle 50% duty cycle <u>3/</u> 100% duty cycle <u>3/</u>	1,2,3	All	5 70 140 300	50 220 375 750	mA
Supply current <u>7/</u>	I _{CCC}	Standby or transmitting	1,2,3	All	5	60	mA
Supply current <u>8/</u>	I _{CCD}	Standby or transmitting	1,2,3	01	10	750	μA
RECEIVER							
Differential input <u>2/</u> impedance	Z _{INDIFF}	Measured through transformer (stub coupled) in accordance with MIL-STD-1553	4,5,6	All	1		kΩ
Input threshold	V _{TH1}	Transformer coupled, (across 70Ω load)	4,5,6	All		0.86	Vp-p
Input threshold <u>3/</u>	V _{TH2}	Direct coupled, (across 35Ω load)	4,5,6	All		1.2	Vp-p
Common mode voltage <u>3/</u>	V _{CM}	Measured through transformer in accordance with MIL-STD-1553	4,5,6	All		±10	V
TRANSMITTER							
Differential output voltage	V _{ODIFF1}	Transformer coupled, (across 70Ω load)	4,5,6	All	20	27	Vp-p
Differential output voltage <u>3/</u>	V _{ODIFF2}	Direct coupled, (across 35Ω load)	4,5,6	All	6	9	Vp-p
Output offset	V _{OFF}	Measured 2.5 μs after last zero crossing	4,5,6	All		±250	mV
Output rise and fall times	t _r , t _f	Transformer coupled, (across 70Ω load), 10% to 90% of full waveform pk-pk	9,10,11	All	100	300	ns

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 5

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LOGIC							
ADDRESS valid to \overline{CS} low setup time <u>2/ 9/</u>	t _{d1}	Host write or read to/from RAM or control blocks	9,10,11	01	0		ns
R/ \overline{W} valid to \overline{CS} low setup time <u>2/</u>	t _{d2}	Host write or read to/from RAM or control blocks	9,10,11	01	0		ns
\overline{CS} low to DATA in valid <u>2/</u>	t _{d3}	Host write to RAM or control blocks <u>2/</u>	9,10,11	01		35	ns
\overline{CS} low to \overline{DTACK} low	t _{d4}	Host write or read to/from RAM - no contention <u>2/</u>	9,10,11	01	120	240	ns
		Host write or read to/from RAM - internal controller performing RAM access, BURST pin = high <u>3/</u>			120	690	ns
		Host write or read to/from RAM - internal controller performing RAM access, BURST pin = low <u>3/</u>			0.12	12.0	μs
\overline{DTACK} low to \overline{CS} high hold time <u>2/</u>	t _{d5}	Host write or read to/from RAM or control blocks	9,10,11	01	0	2.0	μs
\overline{DTACK} low to ADDRESS invalid hold time <u>2/ 9/</u>	t _{d6}	Host write or read to/from RAM or control blocks	9,10,11	01	0		ns
\overline{DTACK} low to R/ \overline{W} invalid hold time <u>2/</u>	t _{d7}	Host write or read to/from RAM or control blocks	9,10,11	01	0		ns
\overline{DTACK} low to DATA in invalid hold time <u>2/</u>	t _{d8}	Host write to RAM or control blocks	9,10,11	01	0		ns
\overline{CS} high to \overline{DTACK} high <u>2/</u>	t _{d9}	Host write or read to/from RAM or control blocks	9,10,11	01	40	120	ns
DATA out valid to \overline{DTACK} low	t _{d10}	Host read from RAM or control blocks <u>2/</u>	9,10,11	01	20		ns
\overline{CS} high to DATA out invalid hold time <u>2/</u>	t _{d11}	Host read from RAM or control blocks	9,10,11	01		35	ns
\overline{CS} low to \overline{DTACK} low <u>2/</u>	t _{d12}	Host write or read to/from control blocks	9,10,11	01	90	180	ns

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 6

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{DMAREQ}}$ low to $\overline{\text{DMAGNT}}$ low (write)	t ₁	DMA write access 2/	9,10,11	02		3.5	μs
$\overline{\text{DMAGNT}}$ low to $\overline{\text{DMAACK}}$ low	t ₂	DMA write or read access 2/	9,10,11	02		185	ns
$\overline{\text{DMAACK}}$ low to $\overline{\text{DMAGNT}}$ high hold time	t ₃	DMA write or read access 2/	9,10,11	02	0		ns
$\overline{\text{DMAACK}}$ low to R/W output enabled	t ₄	DMA write or read access 2/	9,10,11	02		30	ns
$\overline{\text{DMAACK}}$ low to ADDRESS outputs enabled	t ₅	DMA write or read access 2/	9,10,11	02		35	ns
$\overline{\text{DMAACK}}$ low to DATA outputs enabled	t ₆	DMA write access 2/	9,10,11	02		35	ns
$\overline{\text{DMAACK}}$ low to $\overline{\text{STROBE}}$ low (write)	t ₇	DMA write access 2/	9,10,11	02	110	140	ns
$\overline{\text{STROBE}}$ low pulse width (write)	t ₈	DMA write access 2/	9,10,11	02	235	265	ns
$\overline{\text{STROBE}}$ high to DATA changing (write)	t ₉	DMA write access 2/	9,10,11	02	110	155	ns
Transfer cycle time	t ₁₀	DMA write or read access 2/	9,10,11	02	480	520	ns
$\overline{\text{DMAACK}}$ high to R/W output disabled	t ₁₁	DMA write or read access 2/	9,10,11	02		40	ns
$\overline{\text{DMAACK}}$ high to ADDRESS outputs disabled	t ₁₂	DMA write or read access 2/	9,10,11	02		45	ns
$\overline{\text{DMAACK}}$ high to DATA outputs disabled	t ₁₃	DMA write access 2/	9,10,11	02		45	ns
$\overline{\text{DMAACK}}$ high to next $\overline{\text{DMAREQ}}$ low 2/	t ₁₄	DMA write or read access, BURST pin = high	9,10,11	02	235	830	ns
$\overline{\text{DMAREQ}}$ low to $\overline{\text{DMAGNT}}$ low (read)	t ₁₅	DMA write access 2/	9,10,11	02		15.5	μs

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 7

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{DMAACK}}$ low to $\overline{\text{STROBE}}$ low (read)	t ₁₆	DMA read access 2/	9,10,11	02	47	77	ns
$\overline{\text{STROBE}}$ low to DATA inputs valid	t ₁₇	DMA read access 2/	9,10,11	02		140	ns
$\overline{\text{STROBE}}$ low pulse width (read)	t ₁₈	DMA read access 2/	9,10,11	02	295	330	ns
$\overline{\text{STROBE}}$ high to DATA inputs disabled	t ₁₉	DMA read access 2/	9,10,11	02	0		ns
$\overline{\text{STROBE}}$ high to ADDRESS outputs changing	t ₂₀	DMA read access 2/	9,10,11	02	110	155	ns
$\overline{\text{IOREQ}}/\overline{\text{INTBIT}}$ low to $\overline{\text{IOACK}}/\overline{\text{WPE}}$ low 2/	t ₂₁	I/O write or read cycle	9,10,11	02	0.1	34.4	μs
$\overline{\text{IOACK}}/\overline{\text{WPE}}$ low to R/W input valid	t ₂₂	I/O write or read cycle 2/	9,10,11	02		130	ns
$\overline{\text{IOACK}}/\overline{\text{WPE}}$ low to $\overline{\text{IOREQ}}/\overline{\text{INTBIT}}$ high hold time	t ₂₃	I/O write or read cycle 2/	9,10,11	02	0		ns
$\overline{\text{IOACK}}/\overline{\text{WPE}}$ low to ADDRESS inputs valid	t ₂₄	I/O write or read cycle 2/	9,10,11	02		130	ns
$\overline{\text{IOACK}}/\overline{\text{WPE}}$ low to DATA inputs valid.	t ₂₅	I/O write cycle 2/	9,10,11	02		130	ns
$\overline{\text{IOACK}}/\overline{\text{WPE}}$ low pulse width	t ₂₆	I/O write or read cycle 2/	9,10,11	02	475	525	ns
$\overline{\text{IOACK}}/\overline{\text{WPE}}$ high to R/W input disabled	t ₂₇	I/O write or read cycle 3/	9,10,11	02	0	40	ns
$\overline{\text{IOACK}}/\overline{\text{WPE}}$ low to ADDRESS inputs disabled	t ₂₈	I/O write or read cycle 3/	9,10,11	02	0	40	ns
$\overline{\text{IOACK}}/\overline{\text{WPE}}$ low to DATA inputs disabled	t ₂₉	I/O write cycle 3/	9,10,11	02	0	40	ns
$\overline{\text{IOACK}}/\overline{\text{WPE}}$ low to DATA outputs valid	t ₃₀	I/O read cycle 2/	9,10,11	02	150	215	ns
$\overline{\text{IOACK}}/\overline{\text{WPE}}$ low to $\overline{\text{STROBE}}$ low	t ₃₁	I/O read cycle 2/	9,10,11	02	235	265	ns

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 8

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{STROBE}}$ low pulse width (I/O)	t ₃₂	I/O read cycle <u>2/</u>	9,10,11	02	170	205	ns
$\overline{\text{IOACK/WPE}}$ low to DATA outputs disabled	t ₃₃	I/O read cycle <u>2/</u>	9,10,11	02		45	ns
$\overline{\text{RESET}}$ low pulse width	t _{rst}	16 MHz clock must be running for duration of reset pulse <u>3/</u>	9,10,11	All	250		ns
16 MHz clock timing <u>12/</u>	t _{prd1}	Clock period - typical 62.5 nano-seconds	9,10,11	All	62.494	62.506	ns
Clock high pulse width	t _{hp1}	Duty cycle should be typically 50% <u>12/</u>	9,10,11	All	0.4t _{prd1}	0.6t _{prd1}	ns
16 MHz clock frequency tolerance	f _{tol}	Long term stability <u>12/</u>	9,10,11	All		±100	ppm
Parity zero crossing of last received word to MSINT low	t _{int1}	1553 mode. Interrupt enabled in control block <u>2/</u>	9,10,11	All	8.6	<u>10/</u>	μs
		McAir mode. Interrupt enabled in control block <u>2/</u>			6.1	<u>10/</u>	μs
$\overline{\text{MSINT}}$ low pulse width	t _{pw1}	Interrupt enabled in control block <u>2/</u>	9,10,11	All	225	275	ns
Parity zero crossing of last received word to MCINT low	t _{int2}	1553 mode. Interrupt enabled in control block <u>2/</u>	9,10,11	All	6.8	7.5	μs
		McAir mode. Interrupt enabled in control block <u>2/</u>			4.3	5.0	μs
$\overline{\text{MCINT}}$ and $\overline{\text{SYNC}}$ low pulse width	t _{pw2}	Interrupt enabled in control block <u>11/</u>	9,10,11	All	475	525	ns
Parity zero crossing of last received word to GBR low	t _{int3}	1553 mode. Receive messages	9,10,11	All	6.8	7.5	μs
		<u>2/</u> McAir mode. Receive messages			4.3	5.0	μs
$\overline{\text{GBR}}$ low pulse width	t _{pw3}	Receive messages <u>2/</u>	9,10,11	All	475	525	ns
$\overline{\text{GBR}}$ high to $\overline{\text{DMAREQ}}$ low (start of DMA transfer)	t _{dmr}	Receive messages <u>2/</u>	9,10,11	02	40		ns

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 9

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Parity zero crossing of command word to MCRST low	t _{int4}	1553 mode. Non-broadcast	9,10,11	All	30.0	31.5	μs
		1553 mode. Broadcast			6.9	7.5	μs
		McAir mode. Non-broadcast			27.8	29.0	μs
		McAir mode. Broadcast			4.4	5.0	μs
MCRST low pulse width	t _{pw4}	Reset RT modecode <u>2/</u>	9,10,11	All	475	525	ns
Parity zero crossing of command word to low NBGNT	t _{c1} <u>2/</u>	All modes, (1553/1760/McAir)	9,10,11	All	2.3	2.9	μs
Parity zero crossing of command word to command on CH(15..0)	t _{c2} <u>2/</u>	All modes, (1553/1760/McAir)	9,10,11	All	2.3	2.9	μs
Parity zero crossing of command word to CMD/HEADER high	t _{c3} <u>2/</u>	All modes, (1553/1760/McAir)	9,10,11	All	2.3	2.9	μs
NBGNT low pulse width	t _{c4} <u>2/</u>	All modes, (1553/1760/McAir)	9,10,11	All	475	585	ns
NBGNT low to ILLCMD low	t _{c5} <u>2/</u>	All modes, (1553/1760/McAir)	9,10,11	All	0		μs
NBGNT low to CHKSUMEN low	t _{c6} <u>2/</u>	1760 mode	9,10,11	All	0	1.0	μs
ILLCMD low hold time	t _{c7} <u>2/</u>	All modes, (1553/1760/McAir)	9,10,11	All	1500-t _{c5}		ns
CHKSUMEN low hold time	t _{c8} <u>2/</u>	1760 mode	9,10,11	All	1500-t _{c6}		ns
Parity zero crossing of first data word to data word on CH(15..0)	t _{c9} <u>2/</u>	1760 mode	9,10,11	All	1.5	2.9	μs
Parity zero crossing of first data word to CMD/HEADER low	t _{c10}	1760 mode <u>2/</u>	9,10,11	All	1.5	2.9	μs

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 10

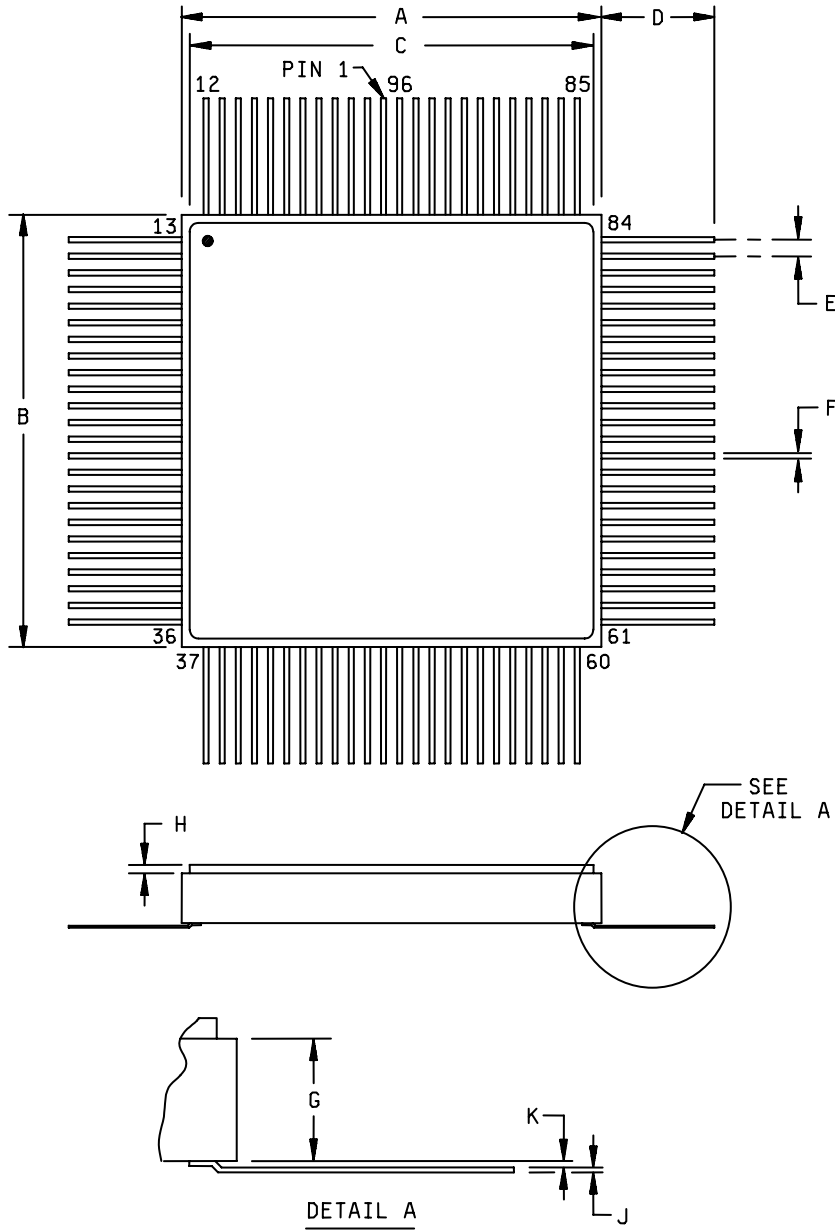
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C +4.5 V dc ≤ V _{CC} ≤ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
<u>CMD/HEADER</u> low to <u>ILLCMD</u> low	t _{c11}	1760 mode <u>2/</u>	9,10,11	All	0	1.0	μs
<u>CMD/HEADER</u> low to <u>CHKSUMEN</u> low	t _{c12}	1760 mode <u>2/</u>	9,10,11	All	0	1.0	μs
<u>ILLCMD</u> low hold time	t _{c13}	1760 mode <u>2/</u>	9,10,11	All	1500-t _{c11}		ns
<u>CHKSUMEN</u> low hold time	t _{c14}	1760 mode <u>2/</u>	9,10,11	All	1500-t _{c12}		ns
Databus response time	t _{resp} <u>2/</u>	1553 mode	9,10,11	All	8.8	9.3	μs
		McAir mode			6.3	6.8	μs
Functional test		Performed to verify functionally in accordance with MIL-STD-1553	7,8	All			Pass/ Fail

- 1/ All group A testing at the same temperature may be performed concurrently.
- 2/ Parameter shall be tested as part of device initial characterization and after any design or process changes and shall be guaranteed to the limits specified in table I.
- 3/ Parameter is not tested but shall be guaranteed by design to the limits to the limits specified in table I. Parameter is listed for information purposes only.
- 4/ Measured at pin functions: RTA0, RTA1, RTA2, RTA3, and RTA4.
- 5/ Measured at pins functions: AIRPRES, CMD/HEADER, and CHKSMFAIL.
- 6 Measured at either the V_{CCA} or the V_{CCB} pin dependent on which bus is transmitting. When the measurement is made the alternate bus is in a standby state.
- 7/ Measured at the V_{CC} pin.
- 8/ Measured at the V_{CCD} pin.
- 9/ When performing a 16 bit transfer the address line A0 is not required. However when performing an 8 bit transfer then A0 is used to indicate the byte to be transferred. A0 = 0 LS byte, A0 = 1 MS byte. Also in 8 bit mode all data is transferred on the LS half of the data bus. D7 - D0.
- 10/ MSINT is generated following transfer of data to/from memory. Hence the maximum time for this parameter is dependent on a number of factors. These include the number of data words in the message, the state of the BURST line, the mode of operation (16 bit or 8 bit), and the extent of subsystem access to the memory.
- 11/ The SYNC interrupt is always available and does not have to be enabled in the control block.
- 12/ Parameter is a requirement on the external clock oscillator. If this is achieved then correct operation of the device is guaranteed.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 11

Case outline X (Device types 01 and 02).



NOTE:

1. The U. S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 12

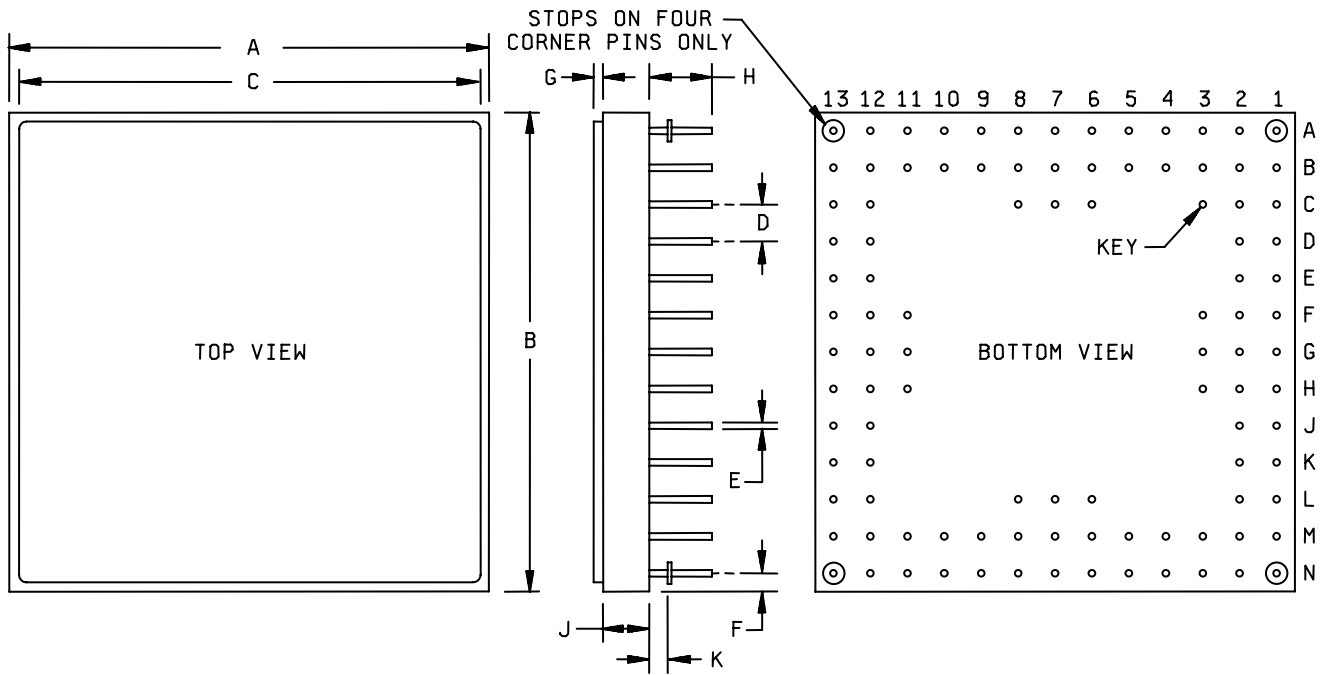
Case outline X (Device types 01 and 02) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	32.69	33.35	1.287	1.313
B	32.69	33.35	1.287	1.313
C	31.57	31.93	1.243	1.257
D	7.77	10.52	.306	.414
E	1.14	1.40	.045	.055
F	0.343	0.495	.0135	.0195
G	3.43	4.19	.135	.165
H	0.58	0.68	.023	.027
J	0.102	0.203	.0040	.0080
K	0.203 TYP		.0080 TYP	

FIGURE 1. Case outline(s) - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 13

Case outline Y (Device types 01 and 02).



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	32.69	33.35	1.287	1.313
B	32.69	33.35	1.287	1.313
C	31.57	31.93	1.243	1.257
D	2.54 TYP		.100 TYP	
E	0.41	0.51	.016	.020
F	1.24	1.30	.049	.051
G	0.58	0.68	.023	.027
H	4.06	4.57	.160	.180
J	2.84	3.51	.112	.138
K	1.14	1.40	.045	.055

NOTE:

- The U. S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s) - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 14

Device types	01		02	
Case outline	X			
Pin number	Pin name	Pin type	Pin name	Pin type
1	TEST1	I	$\overline{\text{INTREG}}$	I
2	$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$	I
3	RREFA	I	RREFA	I
4	GND A	PS	GND A	PS
5	BUS A	I/O	BUS A	I/O
6	V _{CCA}	PS	V _{CCA}	PS
7	$\overline{\text{BUS A}}$	I/O	$\overline{\text{BUS A}}$	I/O
8	$\overline{\text{BUS Y}}$	I	$\overline{\text{BUS Y}}$	I
9	$\overline{\text{SERVREQ}}$	I	$\overline{\text{SERVREQ}}$	I
10	$\overline{\text{SSFLAG}}$	I	$\overline{\text{SSFLAG}}$	I
11	TEST2	I	TEST2	I
12	$\overline{\text{AIRPRES}}$	O	$\overline{\text{AIRPRES}}$	O
13	CH15	O	CH15	O
14	CH14	O	CH14	O
15	CH13	O	CH13	O
16	CH12	O	CH12	O
17	CH11	O	CH11	O
18	CH10	O	CH10	O
19	CH9	O	CH9	O
20	CH8	O	CH8	O

FIGURE 2. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 15

Device types	01		02	
Case outline	X			
Pin number	Pin name	Pin type	Pin name	Pin type
21	SCREEN		SCREEN	
22	C16MHZ	I	C16MHZ	I
23	CH7	O	CH7	O
24	CH6	O	CH6	O
25	CH5	O	CH5	O
26	CH4	O	CH4	O
27	CH3	O	CH3	O
28	CH2	O	CH2	O
29	CH1	O	CH1	O
30	CH0	O	CH0	O
31	$\overline{\text{CMD/HEADER}}$	O	$\overline{\text{CMD/HEADER}}$	O
32	GNDC	PS	GNDC	PS
33	$\overline{\text{ILLCMD}}$	I	$\overline{\text{ILLCMD}}$	I
34	$\overline{\text{CHKSUMEN}}$	I	$\overline{\text{CHKSUMEN}}$	I
35	$\overline{\text{CHKSMFAIL}}$	O	$\overline{\text{CHKSMFAIL}}$	O
36	$\overline{\text{MCINT}}$	O	$\overline{\text{MCINT}}$	O
37	$\overline{\text{MSINT}}$	O	$\overline{\text{MSINT}}$	O
38	$\overline{\text{NBGNT}}$	O	$\overline{\text{NBGNT}}$	O
39	$\overline{\text{SYNC}}$	O	$\overline{\text{SYNC}}$	O
40	$\overline{\text{MCRST}}$	O	$\overline{\text{MCRST}}$	O

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 16

Device types	01		02	
Case outline	X			
Pin number	Pin name	Pin type	Pin name	Pin type
41	$\overline{\text{GBR}}$	O	$\overline{\text{GBR}}$	O
42	$\overline{\text{MEINT}}$	O	$\overline{\text{MEINT}}$	O
43	TEST3	O	$\overline{\text{STROBE}}$	O
44	$\overline{\text{DTACK}}$	O	$\overline{\text{IOACK/WPE}}$	I/O
45	$\overline{\text{CS}}$	I	$\overline{\text{IOREQ/INTBIT}}$	I
46	TEST4	I	$\overline{\text{DMAGNT}}$	I
47	TEST5	O	$\overline{\text{DMAACK}}$	O
48	TEST6	O	$\overline{\text{DMAREQ}}$	O
49	$\overline{\text{BURST}}$	I	$\overline{\text{BURST}}$	I
50	V _{CC}	PS	V _{CC}	PS
51	D0	I/O	D0	I/O
52	D1	I/O	D1	I/O
53	D2	I/O	D2	I/O
54	D3	I/O	D3	I/O
55	D4	I/O	D4	I/O
56	D5	I/O	D5	I/O
57	D6	I/O	D6	I/O
58	D7	I/O	D7	I/O
59	GNDD	PS	GNDD	PS
60	D8	I/O	D8	I/O

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 17

Device types	01		02	
Case outline	X			
Pin number	Pin name	Pin type	Pin name	Pin type
61	D9	I/O	D9	I/O
62	D10	I/O	D10	I/O
63	D11	I/O	D11	I/O
64	D12	I/O	D12	I/O
65	D13	I/O	D13	I/O
66	D14	I/O	D14	I/O
67	D15	I/O	D15	I/O
68	$\overline{R/W}$	I	$\overline{R/W}$	I/O
69	A0	I	A0	I/O
70	A1	I	A1	I/O
71	A2	I	A2	I/O
72	A3	I	A3	I/O
73	V _{CCD}	PS	No connection	
74	A4	I	A4	I/O
75	A5	I	A5	I/O
76	A6	I	A6	I/O
77	A7	I	A7	I/O
78	A8	I	A8	I/O
79	A9	I	A9	I/O
80	A10	I	A10	I/O

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 18

Device types	01		02	
Case outline	X			
Pin number	Pin name	Pin type	Pin name	Pin type
81	A11	I	A11	I/O
82	A12	I	A12	I/O
83	RREFB	I	RREFB	I
84	RTAP	I	RTAP	I
85	RTA4	I	RTA4	I
86	RTA3	I	RTA3	I
87	RTA2	I	RTA2	I
88	RTA1	I	RTA1	I
89	RTA0	I	RTA0	I
90	GNDB	PS	GNDB	PS
91	BUSB	I/O	BUSB	I/O
92	V _{CCB}	PS	V _{CCB}	PS
93	$\overline{\text{BUSB}}$	I/O	$\overline{\text{BUSB}}$	I/O
94	MACMODE	I	MACMODE	I
95	$\overline{\text{MODE1553}}$	I	$\overline{\text{MODE1553}}$	I
96	$\overline{\text{16BITMODE}}$	I	$\overline{\text{16BITMODE}}$	I

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 19

Device types	01		02	
Case outline	Y			
Pin number	Pin name	Pin type	Pin name	Pin type
A1	$\overline{\text{AIRPRES}}$	O	$\overline{\text{AIRPRES}}$	O
A2	TEST2	I	TEST2	I
A3	$\overline{\text{SERVREQ}}$	I	$\overline{\text{SERVREQ}}$	I
A4	$\overline{\text{BUSA}}$	I/O	$\overline{\text{BUSA}}$	I/O
A5	BUSA	I/O	BUSA	I/O
A6	RREFA	I	RREFA	I
A7	TEST1	I	$\overline{\text{INTREG}}$	I
A8	MACMODE	I	MACMODE	I
A9	V _{CCB}	PS	V _{CCB}	PS
A10	GND B	PS	GND B	PS
A11	RTA1	I	RTA1	I
A12	RTA4	I	RTA4	I
A13	RTAP	I	RTAP	I
B1	CH15	O	CH15	O
B2	CH14	O	CH14	O
B3	$\overline{\text{SSFLAG}}$	I	$\overline{\text{SSFLAG}}$	I
B4	$\overline{\text{BUSY}}$	I	$\overline{\text{BUSY}}$	I
B5	V _{CCA}	PS	V _{CCA}	PS
B6	GND A	PS	GND A	PS

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 20

Device types	01		02	
Case outline	Y			
Pin number	Pin name	Pin type	Pin name	Pin type
B7	$\overline{16BITMODE}$	I	$\overline{16BITMODE}$	I
B8	\overline{BUSB}	I/O	\overline{BUSB}	I/O
B9	BUSB	I/O	BUSB	I/O
B10	RTA0	I	RTA0	I
B11	RTA2	I	RTA2	I
B12	RTA3	I	RTA3	I
B13	RREFB	I	RREFB	I
C1	CH12	O	CH12	O
C2	CH13	O	CH13	O
C6	\overline{RESET}	I	\overline{RESET}	I
C7	No connection		No connection	
C8	$\overline{MODE1553}$	I	$\overline{MODE1553}$	I
C12	A12	I	A12	I/O
C13	A11	I	A11	I/O
D1	CH10	O	CH10	O
D2	CH11	O	CH11	O
D12	A10	I	A10	I/O
D13	A9	I	A9	I/O
E1	CH8	O	CH8	O
E2	CH9	O	CH9	O

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 21

Device types	01		02	
Case outline	Y			
Pin number	Pin name	Pin type	Pin name	Pin type
E12	A8	I	A8	I/O
E13	A7	I	A7	I/O
F1	C16MHZ	I	C16MHZ	I
F2	SCREEN		SCREEN	
F3	CH7	O	CH7	O
F11	A4	I	A4	I/O
F12	A6	I	A6	I/O
F13	A5	I	A5	I/O
G1	CH5	O	CH5	O
G2	CH6	O	CH6	O
G3	No connection		No connection	
G11	No connection		No connection	
G12	A3	I	A3	I/O
G13	V _{CCD}	PS	No connection	
H1	CH3	O	CH3	O
H2	CH2	O	CH2	O
H3	CH4	O	CH4	O
H11	A2	I	A2	I/O
H12	A0	I	A0	I/O
H13	A1	I	A1	I/O

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 22

Device types	01		02	
Case outline	Y			
Pin number	Pin name	Pin type	Pin name	Pin type
J1	CH1	O	CH1	O
J2	CH0	O	CH0	O
J12	D15	I/O	D15	I/O
J13	R/W	I	R/W	I/O
K1	CMD/HEADER	O	CMD/HEADER	O
K2	GNDC	PS	GNDC	PS
K12	D13	I/O	D13	I/O
K13	D14	I/O	D14	I/O
L1	ILLCMD	I	ILLCMD	I
L2	CHKSUMEN	I	CHKSUMEN	I
L6	TEST5	O	DMAACK	O
L7	No connection		No connection	
L8	V _{CC}	PS	V _{CC}	PS
L12	D11	I/O	D11	I/O
L13	D12	I/O	D12	I/O
M1	CHKSMFAIL	O	CHKSMFAIL	O
M2	NBGNT	O	NBGNT	O
M3	SYNC	O	SYNC	O
M4	GBR	O	GBR	O
M5	TEST3	O	STROBE	O

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 23

Device types	01		02	
Case outline	Y			
Pin number	Pin name	Pin type	Pin name	Pin type
M6	$\overline{\text{CS}}$	I	$\overline{\text{IOREQ/INTBIT}}$	I
M7	TEST6	O	$\overline{\text{DMAREQ}}$	O
M8	D1	I/O	D1	I/O
M9	D3	I/O	D3	I/O
M10	D5	I/O	D5	I/O
M11	D7	I/O	D7	I/O
M12	D10	I/O	D10	I/O
M13	D9	I/O	D9	I/O
N1	$\overline{\text{MCINT}}$	O	$\overline{\text{MCINT}}$	O
N2	$\overline{\text{MSINT}}$	O	$\overline{\text{MSINT}}$	O
N3	$\overline{\text{MCRST}}$	O	$\overline{\text{MCRST}}$	O
N4	$\overline{\text{MEINT}}$	O	$\overline{\text{MEINT}}$	O
N5	$\overline{\text{DTACK}}$	O	$\overline{\text{IOACK/WPE}}$	I/O
N6	TEST4	I	$\overline{\text{DMAGNT}}$	I
N7	$\overline{\text{BURST}}$	I	$\overline{\text{BURST}}$	I
N8	D0	I/O	D0	I/O
N9	D2	I/O	D2	I/O
N10	D4	I/O	D4	I/O
N11	D6	I/O	D6	I/O
N12	GNDD	PS	GNDD	PS
N13	D8	I/O	D8	I/O

FIGURE 2. Terminal connections - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 24

Device type 01.

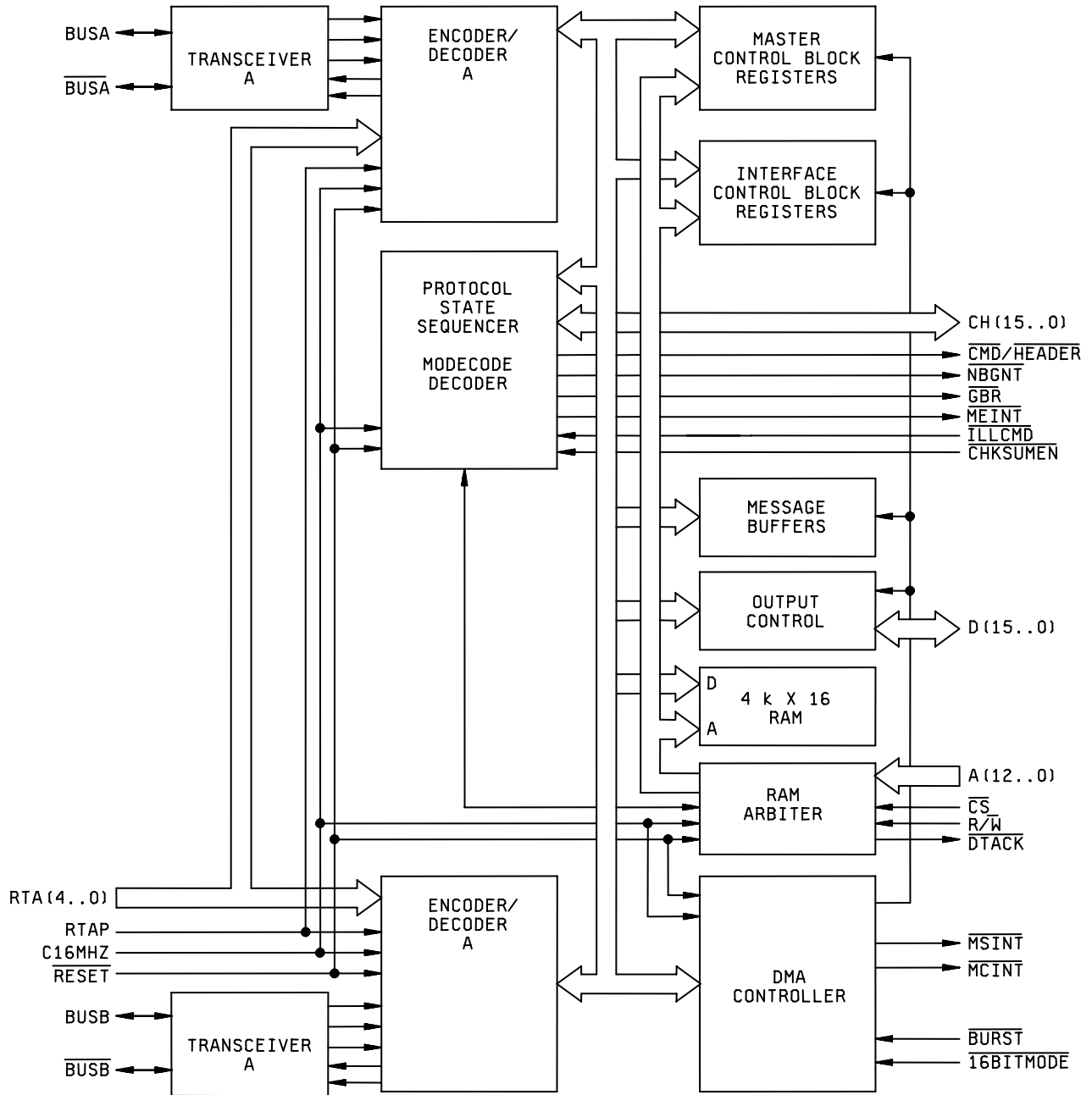


FIGURE 3. Block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 25

Device type 02.

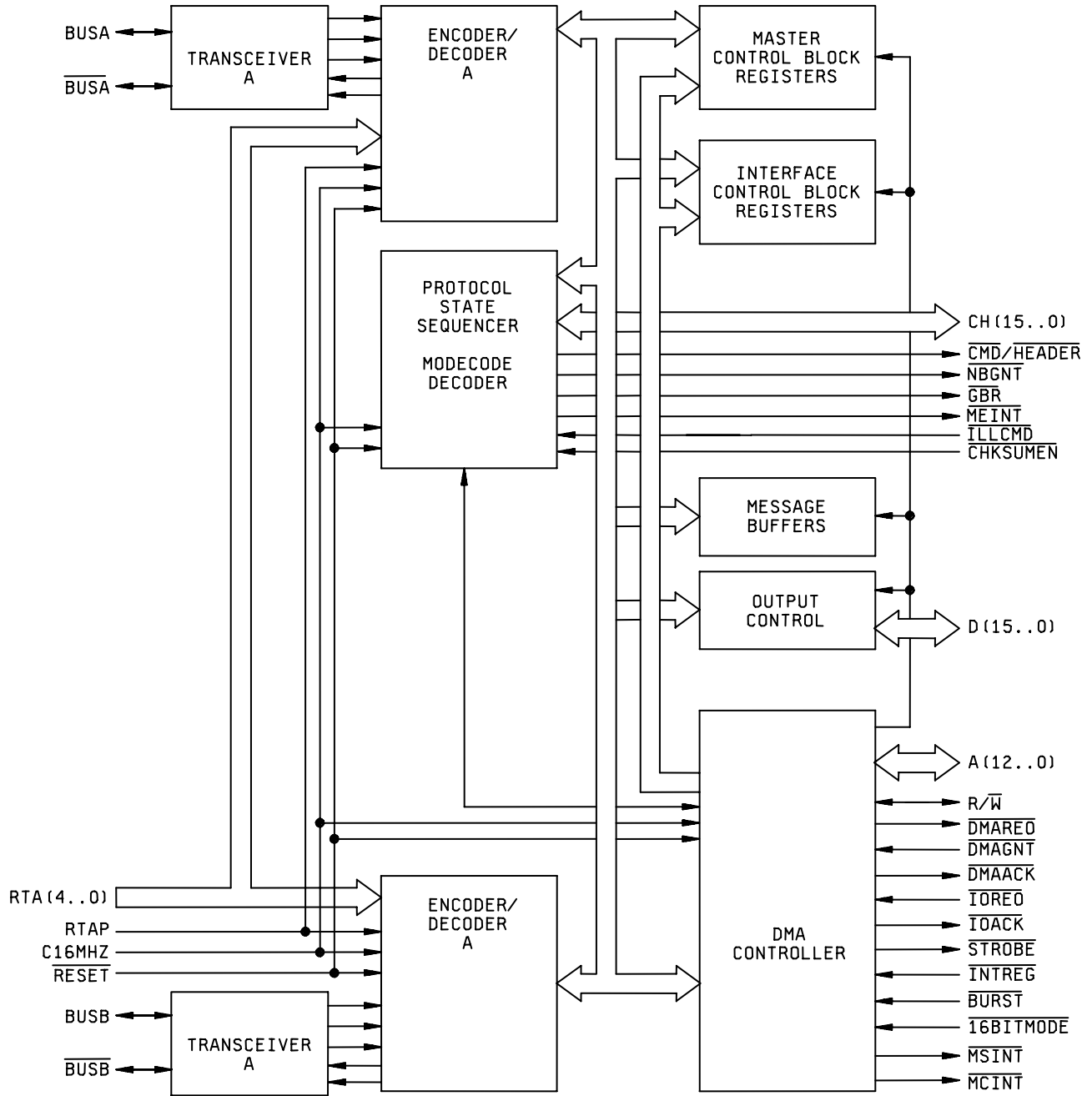
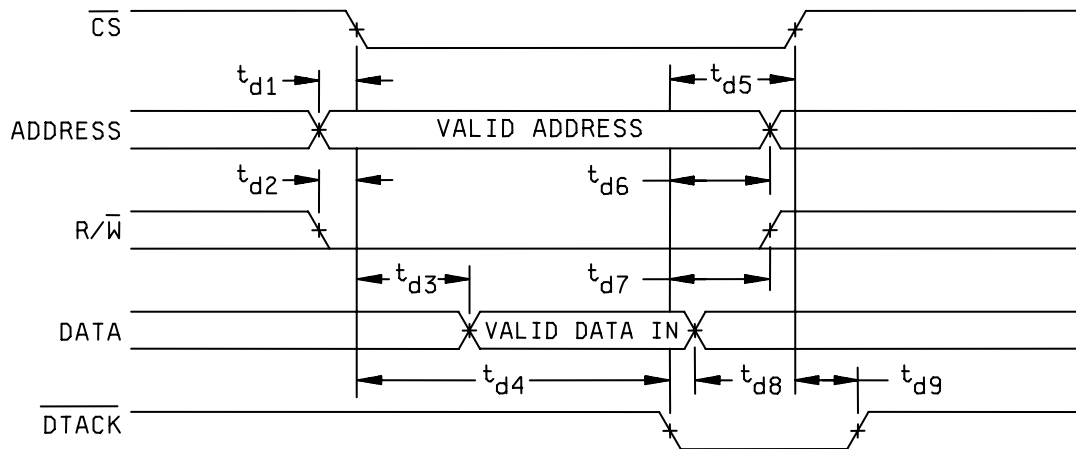
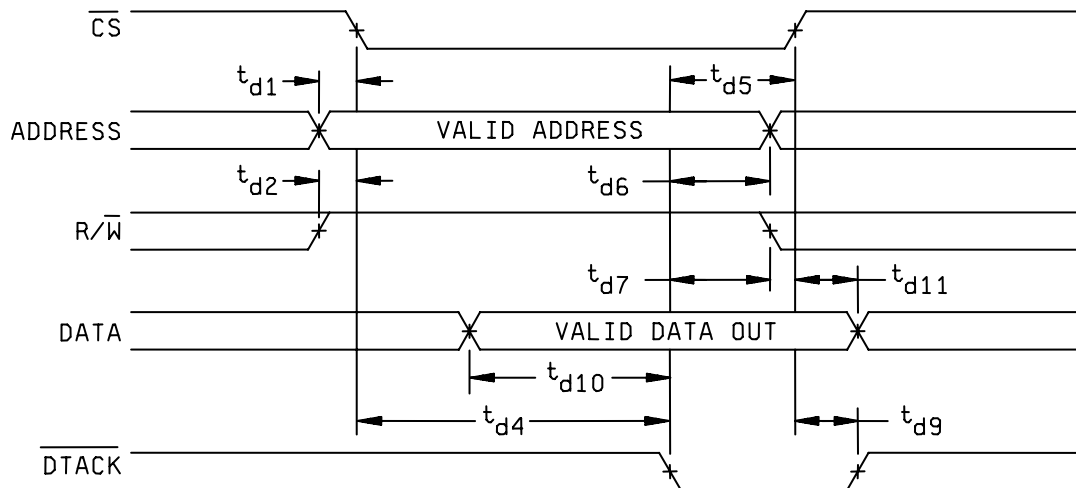


FIGURE 3. Block diagram - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 26



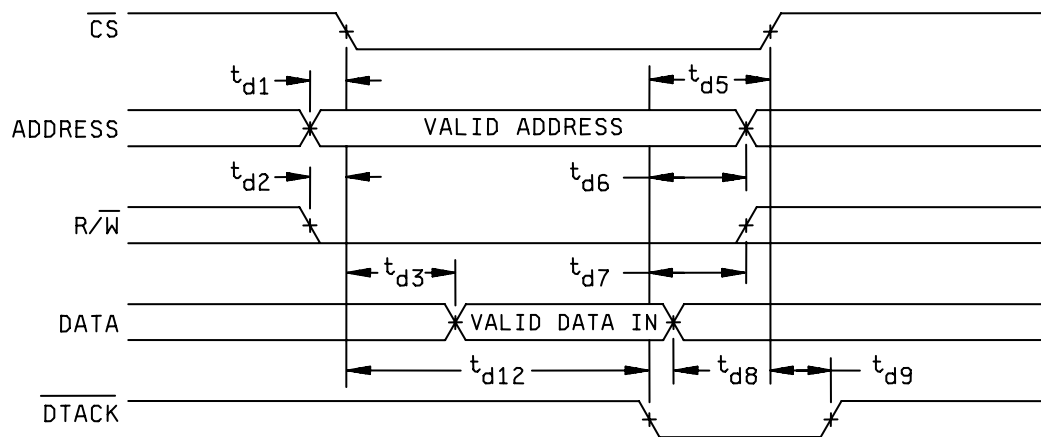
WRITE TO RAM (DEVICE TYPE 01)



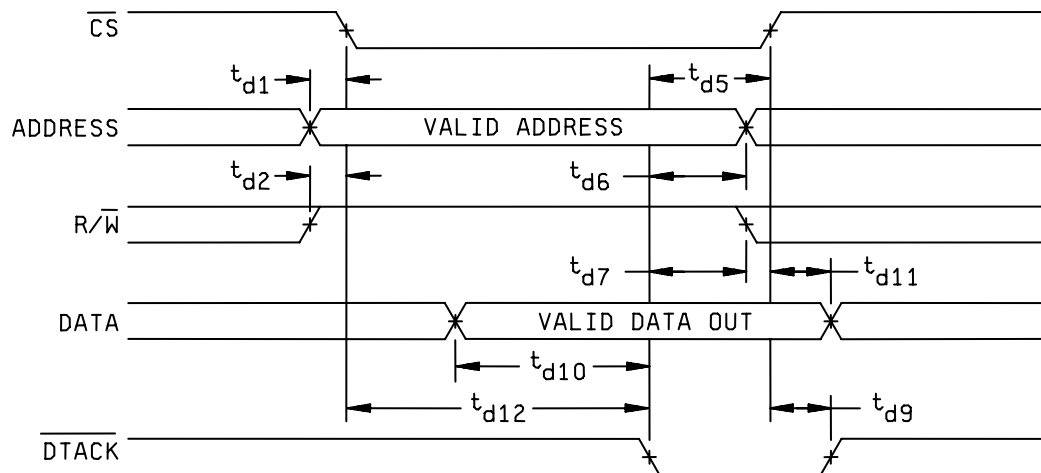
READ FROM RAM (DEVICE TYPE 01)

FIGURE 4. Timing waveforms.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 27



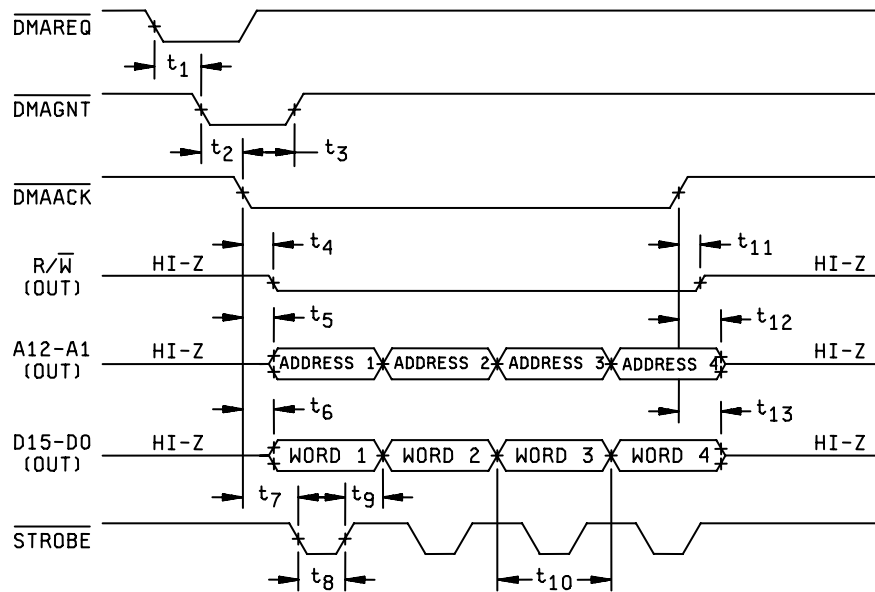
WRITE TO MASTER CONTROL BLOCK OR INTERFACE CONTROL BLOCK (DEVICE TYPE 01)



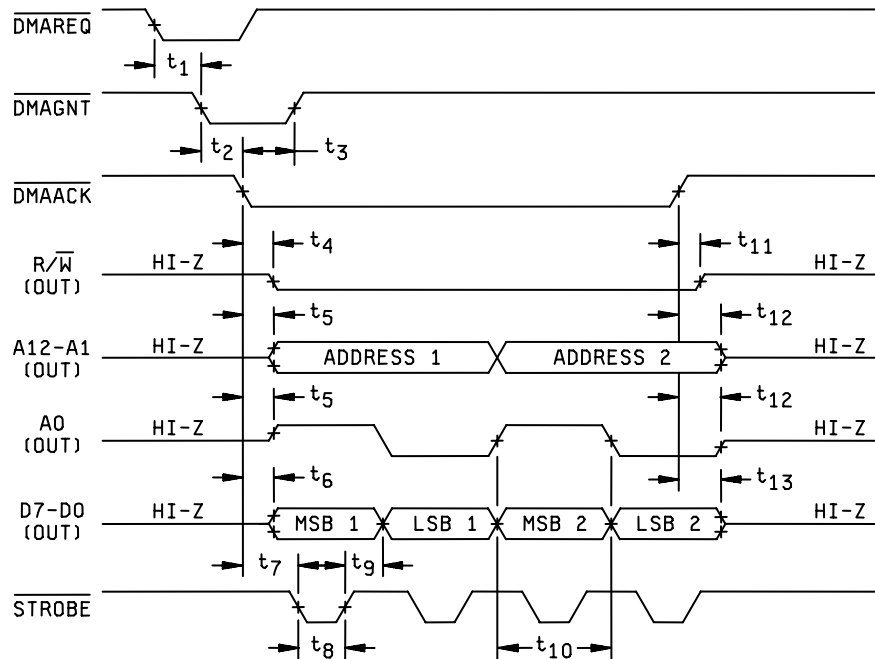
READ FROM MASTER CONTROL BLOCK OR INTERFACE CONTROL BLOCK (DEVICE TYPE 01)

FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 28



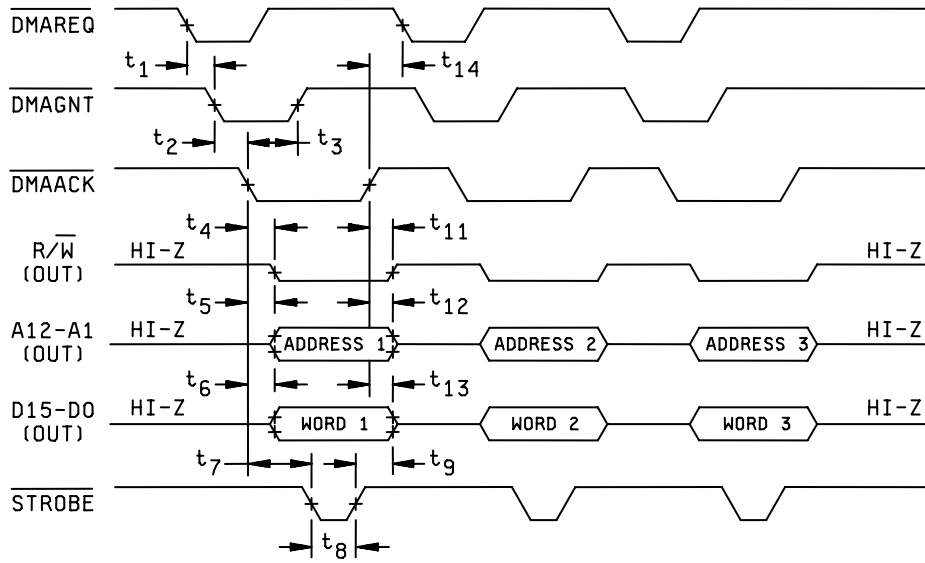
DMA WRITE, BURST MODE, 16 BIT (DEVICE TYPE 02)



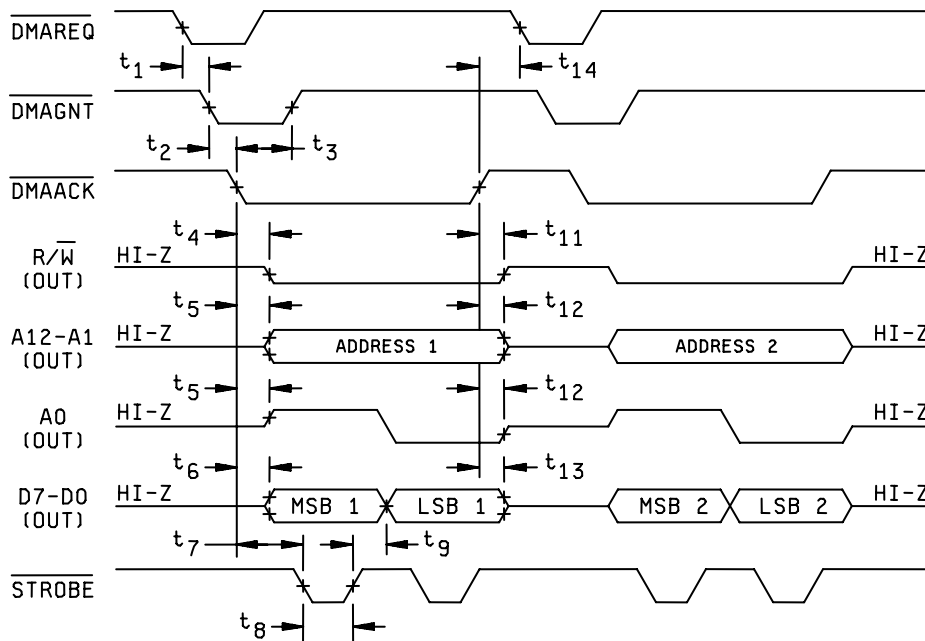
DMA WRITE, BURST MODE, 8 BIT (DEVICE TYPE 02)

FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 29



DMA WRITE, NON-BURST MODE, 16 BIT (DEVICE TYPE 02)



DMA WRITE, NON-BURST MODE, 8 BIT (DEVICE TYPE 02)

FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 30

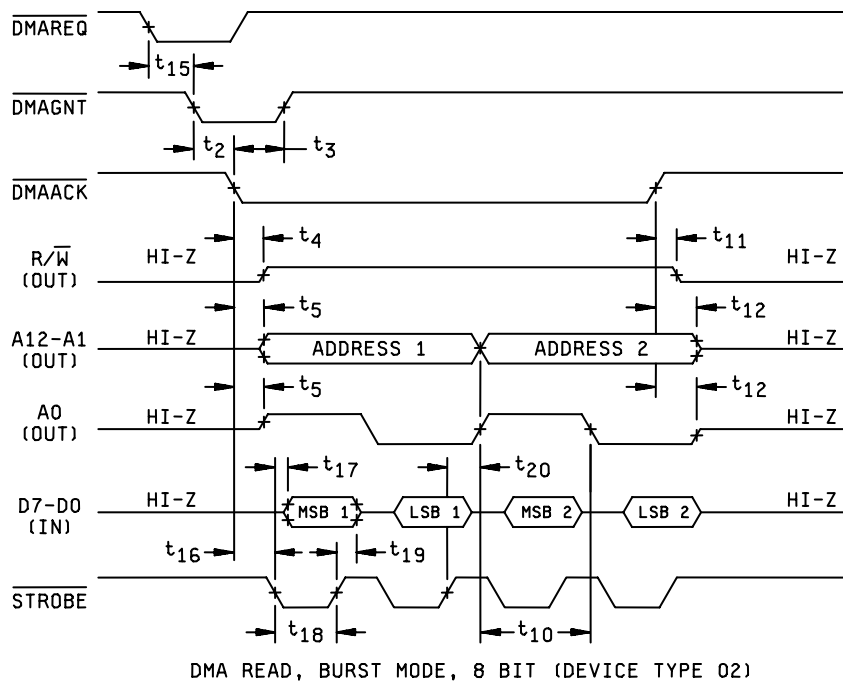
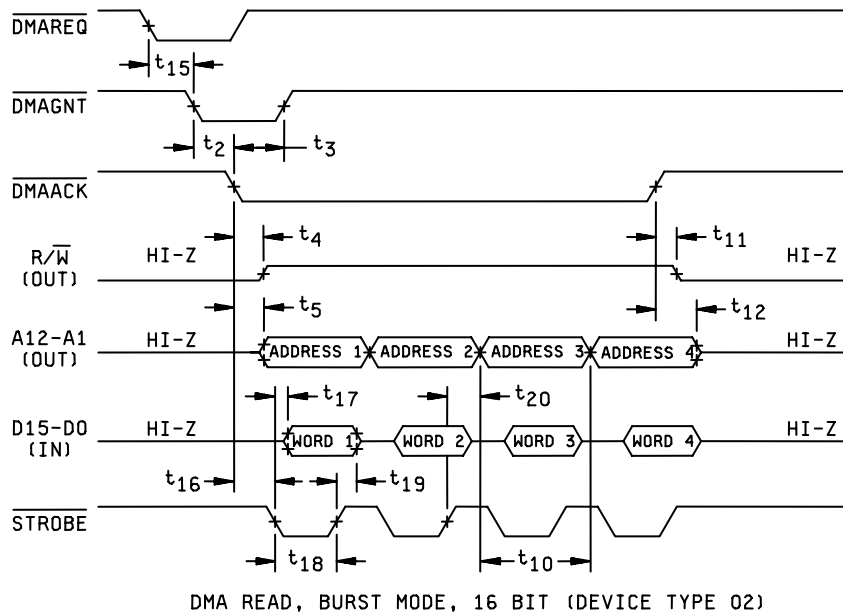


FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 31

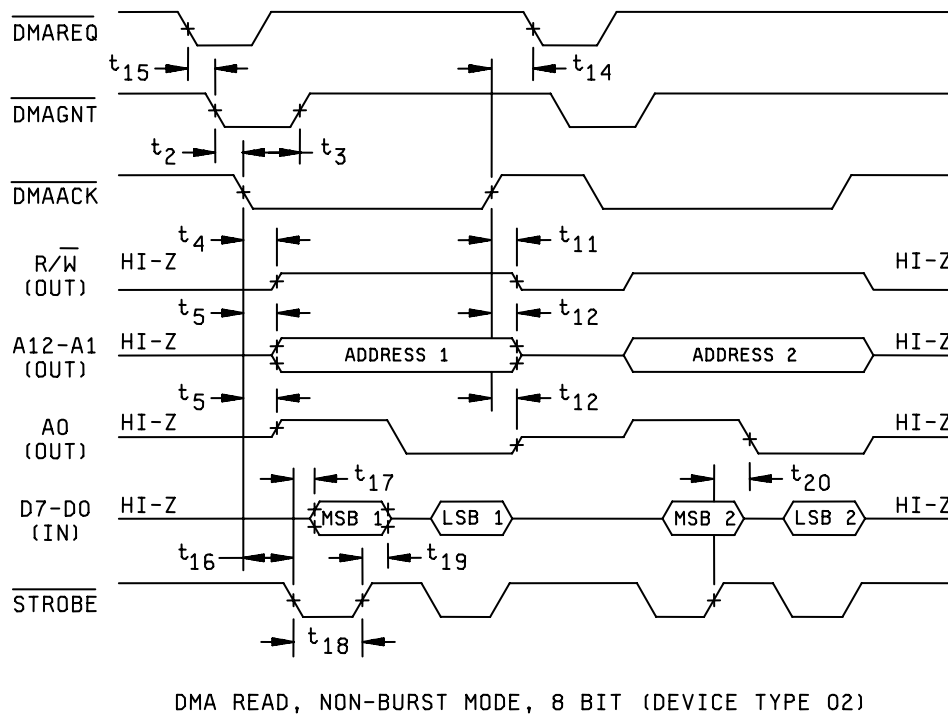
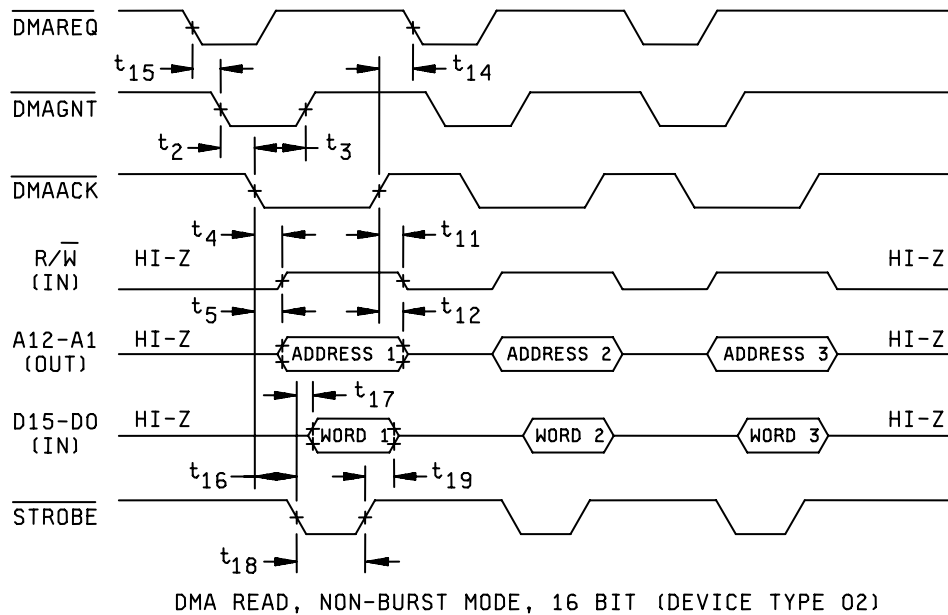
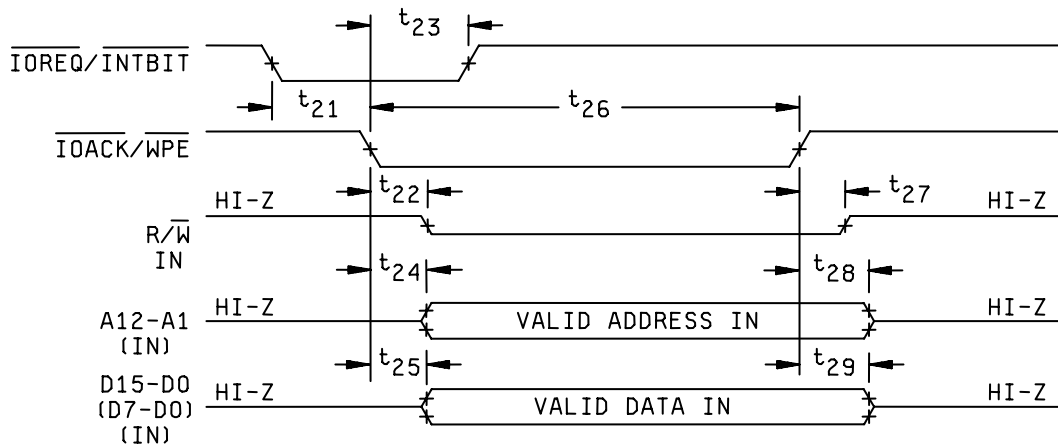
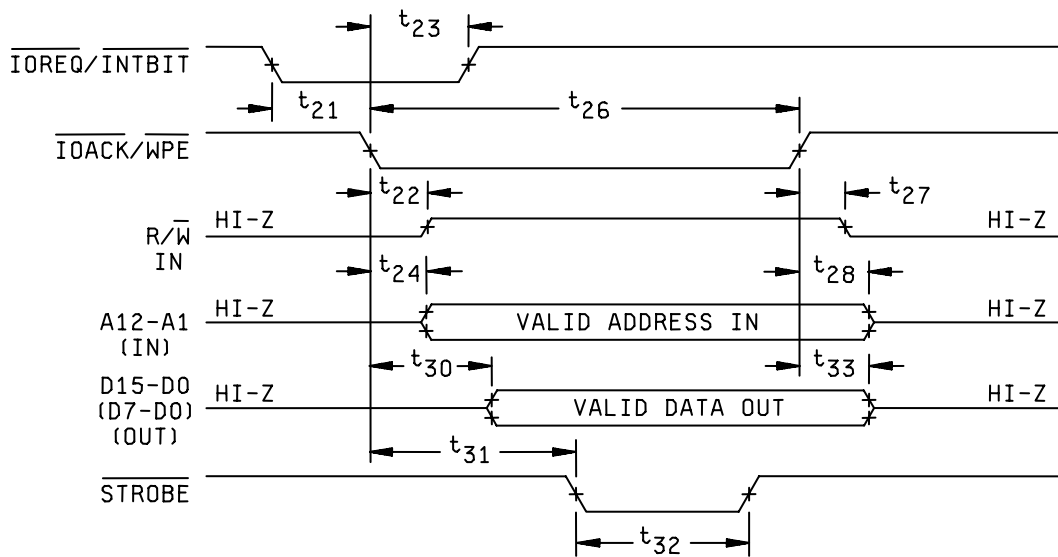


FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 32



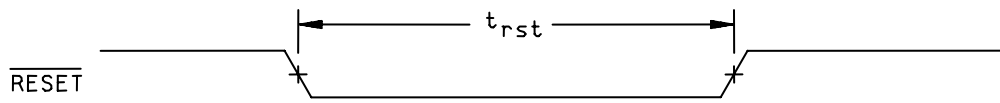
I/O WRITE CYCLE (DEVICE TYPE 02)



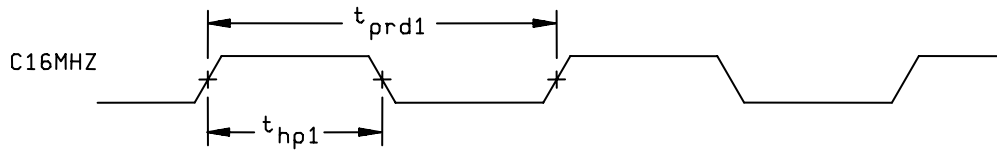
I/O READ CYCLE (DEVICE TYPE 02)

FIGURE 4. Timing waveforms - Continued.

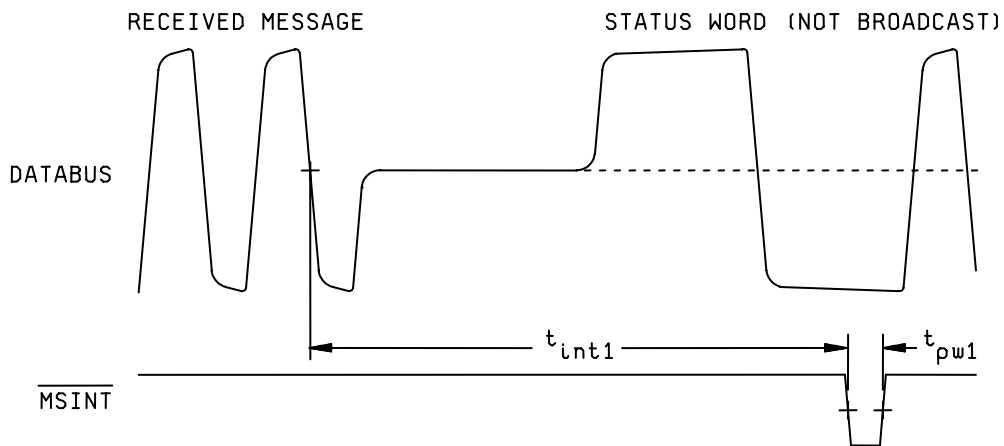
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 33



RESET PULSE TIMING (DEVICE TYPES 01 AND 02)



INPUT CLOCK TIMING (DEVICE TYPES 01 AND 02)



MSINT INTERRUPT TIMING (DEVICE TYPES 01 AND 02)

FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 34

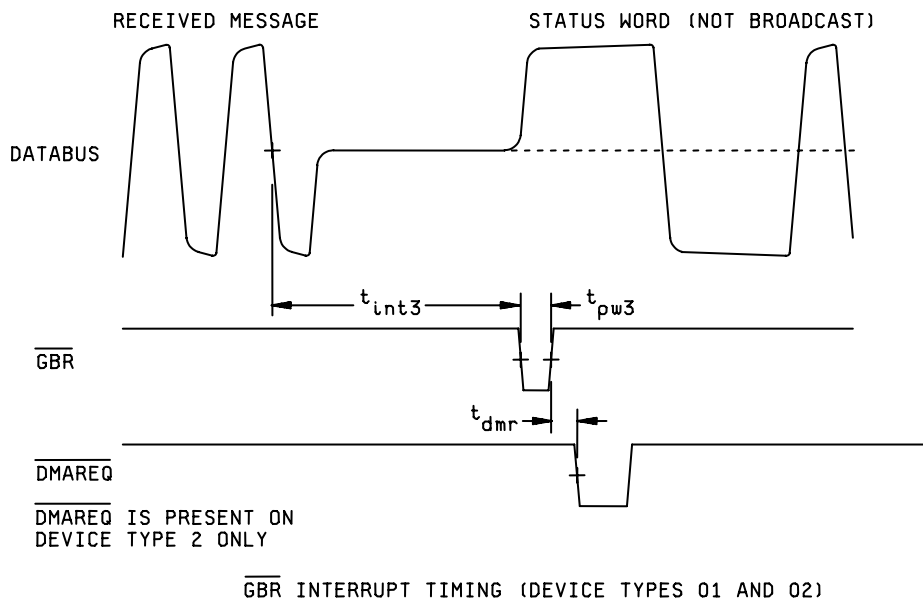
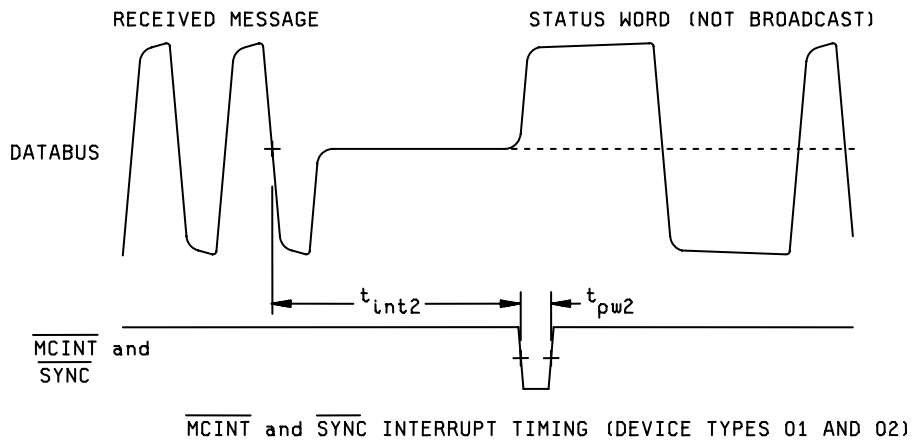
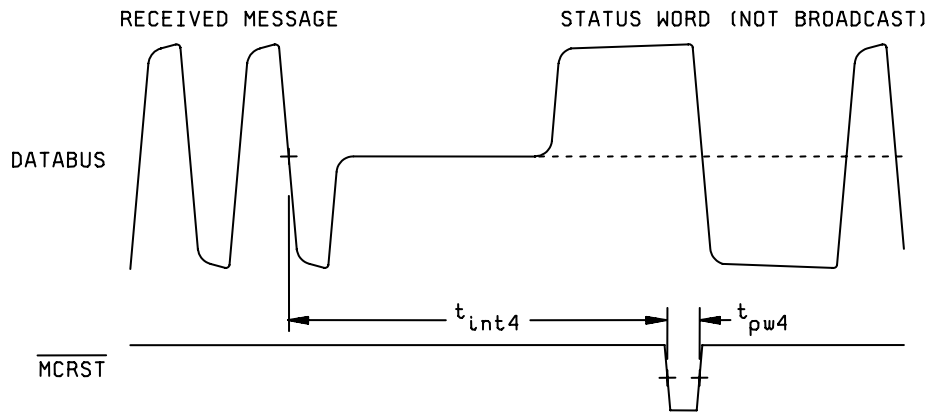
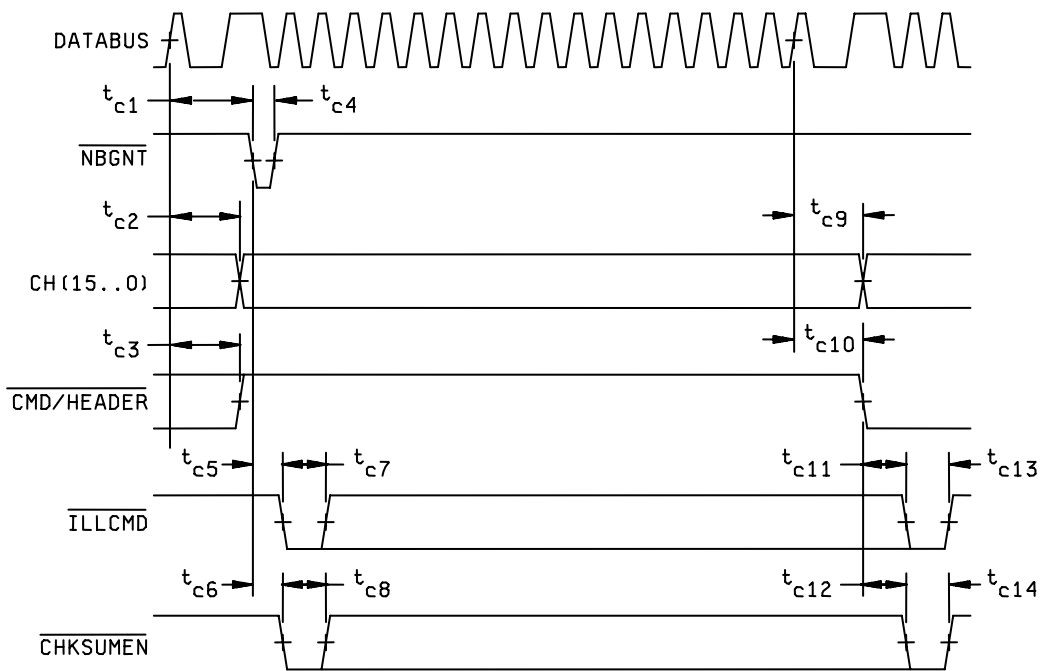


FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 35



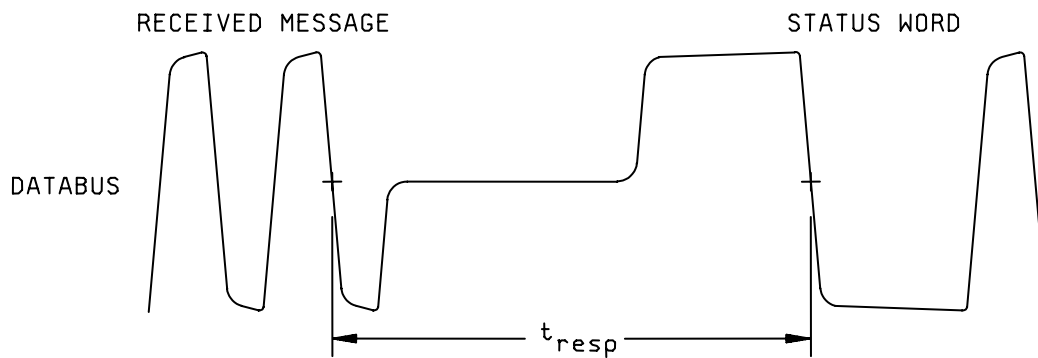
MCRST INTERRUPT TIMING (DEVICE TYPES 01 AND 02)



EXTERNAL COMMAND ILLEGALIZATION AND CHECKSUM CONTROL (DEVICE TYPES 01 AND 02)

FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 36



DATABUS RESPONSE TIMING (DEVICE TYPES 01 AND 02)

FIGURE 4. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 37

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,2,3,4,5,6,9,10,11
Final electrical parameters	1*,2,3,4,5,6,9,10,11
Group A test requirements	1,2,3,4,5,6,9,10,11
Group C end-point electrical parameters	1,2,3,4,5,6,9,10,11
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8A, and 8B shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 38

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Post Office Box 3990, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

6.7 Pin functions. Microcircuits conforming to this drawing shall have pin functions as specified in table III herein.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 39

Table III. Pin functions.

Pin name	Device type	Description
$\overline{16BITMODE}$	All	16/8 bit mode - when high each word is transferred to/from the subsystem as two 8 bit bytes. When low then single 16 bit transfers are used.
A0	All	Host address bus bit 0.
A1	All	Host address bus bit 1.
A2	All	Host address bus bit 2.
A3	All	Host address bus bit 3.
A4	All	Host address bus bit 4.
A5	All	Host address bus bit 5.
A6	All	Host address bus bit 6.
A7	All	Host address bus bit 7.
A8	All	Host address bus bit 8.
A9	All	Host address bus bit 9.
A10	All	Host address bus bit 10.
A11	All	Host address bus bit 11.
A12	All	Host address bus bit 12.
$\overline{AIRPRES}$	All	Aircraft present (active low) - this pin provides an indication as to the status of the store and is derived from the values present on the RT address lines which should be pulled to a logic high when the store separates from the aircraft. This causes AIRPRES to go to a logic high level on store separation.
\overline{BURST}	All	Burst mode (active low) - when low data words associated with a single message are transferred to memory (internal or external) using one DMA request/grant cycle. During the transfer the host is prevented from accessing memory. When this signal is high then separate cycles are used for each word.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 40

Table III. Pin functions - Continued.

Pin name	Device type	Description
BUSA	All	1553 bus A, positive phase signal. This signal should be connected to a bus coupling transformer which should have a turns ratio of 1:2.38 direct, 1:1.67 stub. CMAC FC1760TI or equivalent.
$\overline{\text{BUSA}}$	All	1553 bus A, negative phase signal. This signal should be connected to a bus coupling transformer which should have a turns ratio of 1:2.38 direct, 1:1.67 stub. CMAC FC1760TI or equivalent.
BUSB	All	1553 bus B, positive phase signal. This signal should be connected to a bus coupling transformer which should have a turns ratio of 1:2.38 direct, 1:1.67 stub. CMAC FC1760TI or equivalent.
$\overline{\text{BUSB}}$	All	1553 bus B, negative phase signal. This signal should be connected to a bus coupling transformer which should have a turns ratio of 1:2.38 direct, 1:1.67 stub. CMAC FC1760TI or equivalent.
$\overline{\text{BUSY}}$	All	Busy bit (active low) - setting this line to a low level will cause the BUSY bit to be set in the MIL-STD-1553 status word. This remains true until the line is returned high. If a message requests the transmission of data words the response will be truncated after the transmission of the status word.
C16MHZ	All	16 MHz clock signal.
CH0	All	Command/Header bus bit 0.
CH1	All	Command/Header bus bit 1.
CH2	All	Command/Header bus bit 2.
CH3	All	Command/Header bus bit 3.
CH4	All	Command/Header bus bit 4.
CH5	All	Command/Header bus bit 5.
CH6	All	Command/Header bus bit 6.
CH7	All	Command/Header bus bit 7.
CH8	All	Command/Header bus bit 8.
CH9	All	Command/Header bus bit 9.
CH10	All	Command/Header bus bit 10.
CH11	All	Command/Header bus bit 11.
CH12	All	Command/Header bus bit 12.
CH13	All	Command/Header bus bit 13.
CH14	All	Command/Header bus bit 14.
CH15	All	Command/Header bus bit 15.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 41

Table III. Pin functions - Continued.

Pin name	Device types	Description
$\overline{\text{CHKSMFAIL}}$	All	Checksum failure (active low) - this signal is used in MIL-STD-1760 mode only and indicates that the checksum value received as the last word of a message did not comply with the requirements of the specified checksum algorithm.
$\overline{\text{CHKSUMEN}}$	All	Checksum enable (active low) - this signal is used in MIL-STD-1760 mode only and causes activation of the checksum generation/validation circuitry.
$\overline{\text{CMD/HEADER}}$	All	Command/Header - this signal is used in MIL-STD-1760 mode only and indicates the presence of either the command word (when high) or the header word (when low) on the Command/Header bus.
$\overline{\text{CS}}$	01	Chip select (active low) - this signal is driven low by the host to enable access to the device memory.
D0	All	Host data bus bit 0.
D1	All	Host data bus bit 1.
D2	All	Host data bus bit 2.
D3	All	Host data bus bit 3.
D4	All	Host data bus bit 4.
D5	All	Host data bus bit 5.
D6	All	Host data bus bit 6.
D7	All	Host data bus bit 7.
D8	All	Host data bus bit 8.
D9	All	Host data bus bit 9.
D10	All	Host data bus bit 10.
D11	All	Host data bus bit 11.
D12	All	Host data bus bit 12.
D13	All	Host data bus bit 13.
D14	All	Host data bus bit 14.
D15	All	Host data bus bit 15.

**STANDARD
MICROCIRCUIT DRAWING**

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-95539

REVISION LEVEL
A

SHEET
42

Table III. Pin functions - Continued.

Pin name	Device types	Description
$\overline{\text{DMAACK}}$	02	DMA data transfer acknowledge (active low) - this signal is driven low to the subsystem to indicate that the DMA transfer is in progress and will remain low until the transfer is complete.
$\overline{\text{DMAGNT}}$	02	DMA data transfer grant (active low) - this signal is driven low by the subsystem to indicate that the request made by the RT for initiation of a DMA transfer has been granted. Once the transfer has started ($\overline{\text{DMAACK}}$ driven low) then $\overline{\text{DMAGNT}}$ can be returned high.
$\overline{\text{DMAREQ}}$	02	DMA data transfer request (active low) - this signal is driven low to the subsystem to indicate that the RT requires to transfer data to or from external circuitry. It will be returned on receipt of the grant signal ($\overline{\text{DMAGNT}}$ driven high).
$\overline{\text{DTACK}}$	01	Host data transfer acknowledge (active low) - this signal indicates to the host that a data transfer has been completed. When the host is reading data $\overline{\text{DTACK}}$ will be taken low to signal that data is on the bus stable. $\overline{\text{DTACK}}$ will not be taken back high until CS is returned to a high level.
$\overline{\text{GBR}}$	All	Good block received (active low) - this is a 500 ns negative going pulse used to indicate to the host that a complete valid receive message has been stored in one of the internal message buffers and is about to be transferred to the memory (internal or external).
GNDA	All	Power supply return connection - transceiver A.
GNDB	All	Power supply return connection - transceiver B.
GNDC	All	Power supply return connection - logic circuitry.
GNDD	All	Power supply return connection - logic circuitry.
$\overline{\text{ILLCMD}}$	All	Illegal command - this signal is driven low following receipt of a 1553 command to indicate that it is illegal. It can also be used in MIL-STD-1760 mode to indicate that a received command/header word combination is invalid.
$\overline{\text{INTREG}}$	02	Internal register select (active low) - when low this signal allows access to the internal registers through the use of I/O transfers. If high then the internal registers are not accessible and the data words associated with the transmit vector word and synchronize with data modecodes are transferred to/from subsystem memory using DMA cycles.
$\overline{\text{IOREQ/INTBIT}}$	02	I/O data transfer request/internal BIT register select (active low) - this pin has two functions depending on the state of the INTREG line. If INTREG is low then it is used to initiate a subsystem I/O transfer to one of the RT internal registers. If INTREG is high then register access is disabled and this line is used to specify that the data word associated with a transmit bit word modecode should be read from subsystem memory using a DMA cycle.

**STANDARD
MICROCIRCUIT DRAWING**

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-95539

REVISION LEVEL
A

SHEET
43

Table III. Pin functions - Continued.

Pin name	Device types	Description
$\overline{\text{IOACK/WPE}}$	02	I/O data transfer acknowledge / Wraparound Enable (active low) - this pin has two functions depending on the state of the INTREG line. If INTREG is low then it is driven low to the subsystem to indicate that a request to start an I/O cycle (IOREQ low) has been granted. If INTREG is high then register access is disabled and this line is used to control the wraparound function. If low then internal wraparound (within the RT) is enabled for messages to subaddress 30.
MACMODE	All	McAir mode - If connected to a high level then the device is put into McAir compatible mode. In this mode the response time is less than 7 μs and the RT regards subaddress 31 as a normal subaddress rather than a modecode indicator.
$\overline{\text{MCINT}}$	All	Modecode Interrupt (active low) - if programmed in the control block then this line is used to generate a 500 ns negative going pulse indicating to the host that a specified modecode has been received over the 1553 bus.
$\overline{\text{MCRST}}$	All	Reset RT Modecode Interrupt (active low) - This is a 500 ns negative going pulse indicating to the host that a reset RT modecode had been received over the 1553 bus. For non-broadcast commands the pulse is generated following transmission of the complete 1553 status word.
$\overline{\text{MEINT}}$	All	Message Error Interrupt (active low) - this is a 500 ns negative going pulse indicating to the host that the message currently being received is invalid. Any data received with it will not be transferred to memory (internal or external).
$\overline{\text{MSINT}}$	All	Message Interrupt (active low) - if programmed in the control block then this line is used to generate a 250 ns negative going pulse indicating to the host that a specified message has been received over the 1553 bus and any data associated with it has been transferred to/from memory (internal or external).
$\overline{\text{MODE1553}}$	All	MIL-STD-1553 mode enable (active low) - when low and (MACMODE is low) then the RT will operate in standard MIL-STD-1553 mode. If this line is connected to a high level and (MACMODE is low) then the extra functions associated with MIL-STD-1760 are activated. These include checksum generation and validation, header word illegalization and message limiting to 30 words.
$\overline{\text{NBGNT}}$	All	New Bus Grant (active low) - this is a 500 ns negative going pulse indicating to the host that a new valid command has been received over the 1553 bus and is now available on the Command/Header bus.
$\overline{\text{RESET}}$	All	Reset (active low) - when driven low the entire RT is reset to a power up state. The 16 MHz clock must be running and the reset pulse must have a width of at least 250 ns.
RREFA	All	Receiver reference voltage transceiver A - this is a factory test point and must be left unconnected.
RREFB	All	Receiver reference voltage transceiver B - this is a factory test point and must be left unconnected.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-95539
		REVISION LEVEL A	SHEET 44

Table III. Pin functions - Continued.

Pin name	Device types	Description
RTA0	All	RT address bus bit 0.
RTA1	All	RT address bus bit 1.
RTA2	All	RT address bus bit 2.
RTA3	All	RT address bus bit 3
RTA4	All	RT address bus bit 4.
RTAP	All	RT address bus parity bit - this line must be set to indicate the state of the 5 RT address lines RT0-RT4 using odd parity.
R/\overline{W}	All	Read/Write - this signal controls the direction of data transfer to or from the subsystem. For device type 01 this signal is an input only and when low indicates that data is to be transferred from the host to the RT. When high data is transferred in the opposite direction. For device type 02 the signal is bi-directional and is used for both DMA and I/O transfers. With I/O transfers it works the same way as described above, however for DMA transfers it indicates the opposite, i.e. when low, data is transferred from the RT to the host, and when high it is transferred from the host to the RT.
SCREEN	All	Package screen connection - this pin electrically connected to the lid of the package.
$\overline{\text{SERVREQ}}$	All	Service Request Bit (active low) - setting this line to a low level will cause the SERVICE REQUEST bit to be set in the MIL-STD-1553 status word. This remains true until the line is returned high.
$\overline{\text{SSFLAG}}$	All	Subsystem Flag bit (active low) - setting this line to a low level will cause the SUBSYSTEM FLAG bit to be set in the MIL-STD-1553 status word. This remains true until the line is returned high.
$\overline{\text{STROBE}}$	02	Data transfer strobe (active low) - this signal is activated during DMA write and read transfers and can be used by the host to strobe the data into or out of external memory devices. It is also activated during I/O read cycles for the same purpose.
SYNC	All	Synchronize modecode Interrupt (active low) - this is a 500 ns negative going pulse indicating to the host that one of the two synchronize modecodes (with or without data) has been received.
TEST1, TEST4	01	Factory test input - connect to 0 V.
TEST2	All	Factory test input - for device type 01 connect this to 0 V, and for device type 02 connect to +5 V.
TEST3, TEST5, TEST6	01	Factory test output - do not connect.
V_{CCA}	All	Power supply +5 V connection - transceiver A.
V_{CCB}	All	Power supply +5 V connection - transceiver B.
V_{CCC}	All	Power supply +5 V connection - logic circuitry.
V_{CCD}	01	Power supply +5 V connection - logic circuitry.

**STANDARD
MICROCIRCUIT DRAWING**

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-95539

REVISION LEVEL
A

SHEET
45

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-07-26

Approved sources of supply for SMD 5962-95539 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DSCC maintains an online database of all current sources of supply at <http://www.dsccl.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9553901HXX	U4388	<u>3/</u>
5962-9553901HYC	U4388	RTM1760-PGA
5962-9553902HXX	U4388	<u>3/</u>
5962-9553902HYC	U4388	RTS1760-PGA

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Case outline X is not available by the specified vendor at this time.

Vendor CAGE number

U4388

Vendor name and address

C-MAC Microelectronics Limited
 South Denes
 Great Yarmouth
 Norfolk NR30 3PX
 England

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.